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PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

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Application Number	09/874,367 ✓
Filing Date	June 6, 2001
First Named Inventor	Yoshiyuki TANI
Group Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	0819-0568
Total Number of Pages in This Submission	

ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an Application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input checked="" type="checkbox"/> Preliminary Amendment
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Signature	
Date	November 8, 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Yoshiyuki TANI) Attention: Applications Branch
Serial No. 09/874,367)
Filed: June 6, 2001)
For: PHOTOMASK FORMATION)
METHOD AND ALIGNMENT)
METHOD)

#31A
2/4/02
Hays

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents

Washington, D.C. 20231

Sir:

Please preliminary amend the above-identified application as follows:

IN THE SPECIFICATION

Please amend the specification as follows:

On Page 7, Paragraph 2

As shown in FIG. 11B, the on-wafer intended pattern 132 (gate pattern) has already been defined for the reference layer by the isolation film 131 and wafer surface in the on-wafer intended pattern region 171. An on-wafer intended pattern 183 is going to be formed for the layer-to-be-aligned on the on-wafer intended pattern 132 so that gate electrodes will be arranged three by three at a width of 0.5 μm and a space of 0.5 μm . For that purpose, the mask is automatically aligned by reference to the on-wafer alignment marks 134 for the reference layer shown in FIG. 9A. Thereafter, the photoresist film 182 is exposed and developed and thereby defining a resist pattern for forming the gate electrodes, alignment accuracy measuring marks (see the parts indicated by broken lines) and alignment marks for the next process step, for example.